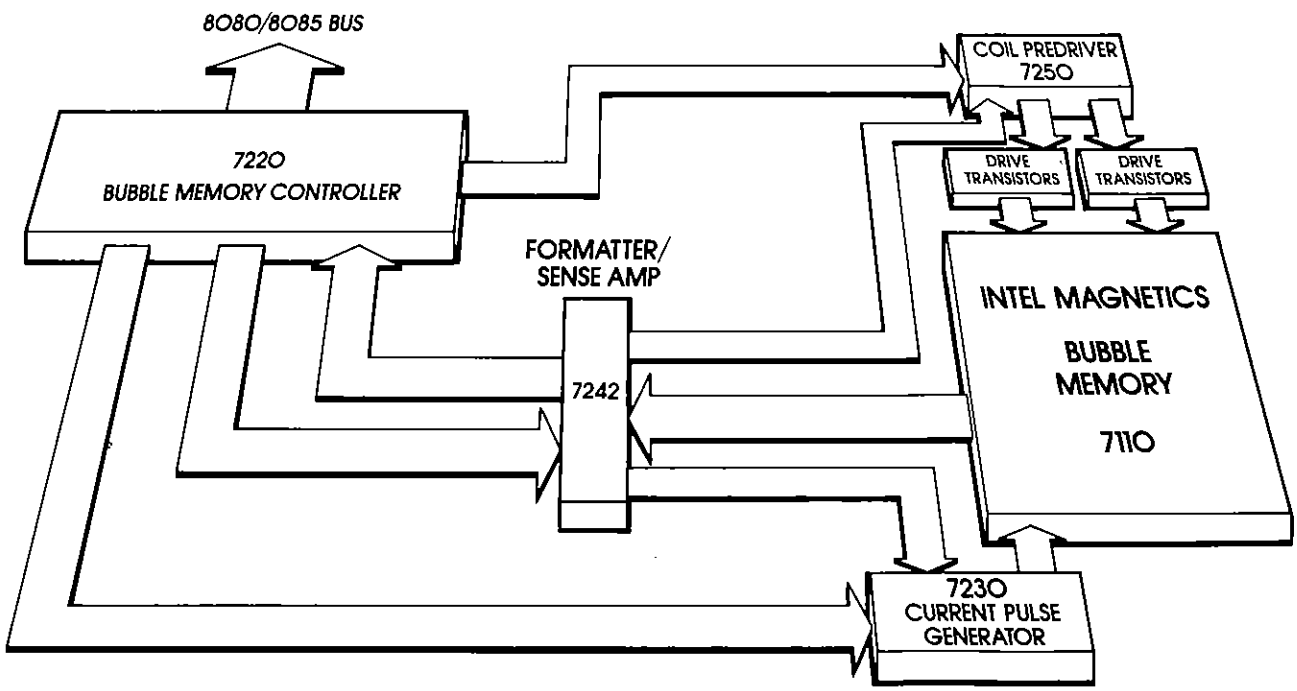
7254
QUAD VMOS DRIVE TRANSISTORS FOR BUBBLE MEMORIES

Features

- Designed to Drive X and Y Coils of IM's Bubble Memories
- No Bias Currents Required
- Fast Turn-on and Turn-off — 30ns Maximum
- Built-in Diode Commutates Coil Current when Transistor is Turned Off
- Operates from V_{DD} Only
- VMOS FET Technology
- N-Channel and P-Channel Transistors on the Same Chip
- Standard 14-Pin Dual-In-Line Package

Description

The 7254 is a quad transistor pack designed to drive the X and Y coils of Intel Magnetics Bubble Memories. Two 7254 packages are required for each bubble memory device. In a typical application D1 and D4 of a 7254 would be connected to an X input of the bubble memory and D2 and D3 would be connected to a Y input. S1 and S3 are grounded and S2 and S4 are tied to V_{DD}.

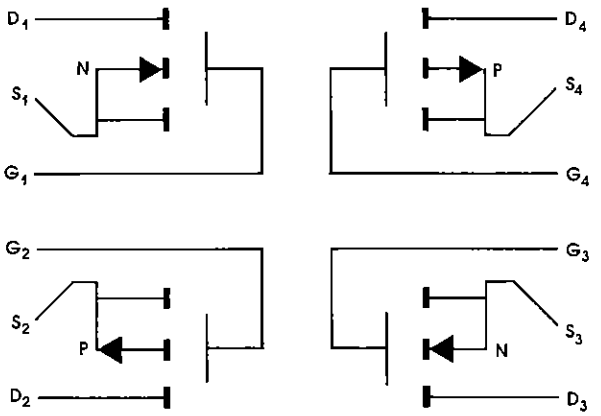


Block Diagram of Single Bubble Memory System — 128K Bytes

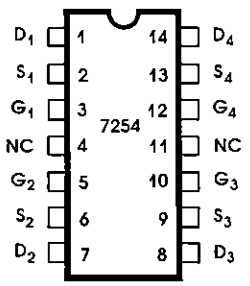
Preliminary

7254

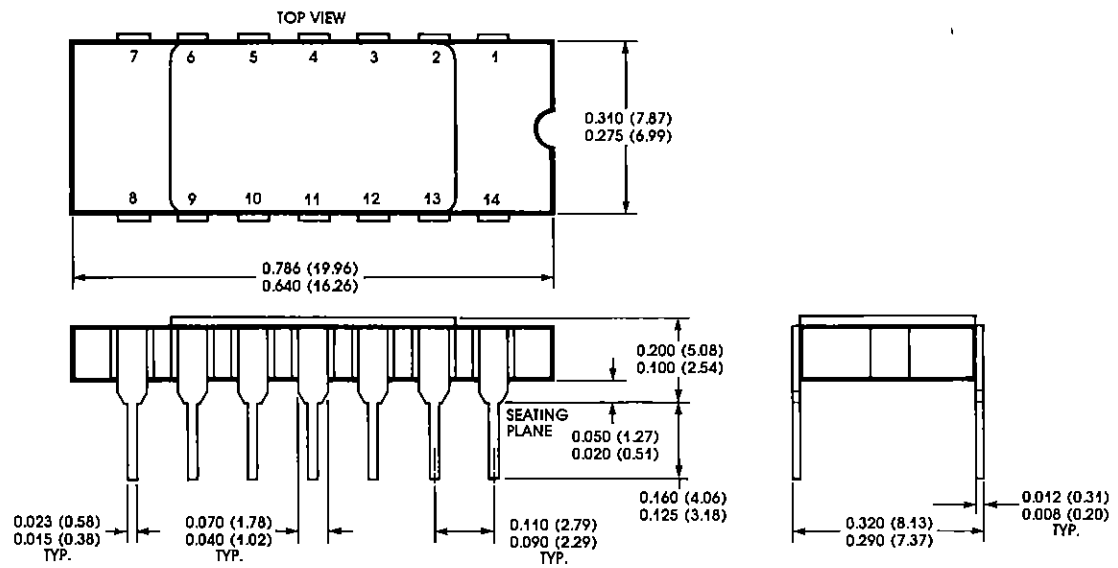
Circuit Diagram



Pin Configuration



Packaging Information



D.C. and Operating Characteristics

All Limits Apply for N- and P-Channel transistors, T_A=0 to 70°C unless otherwise noted.

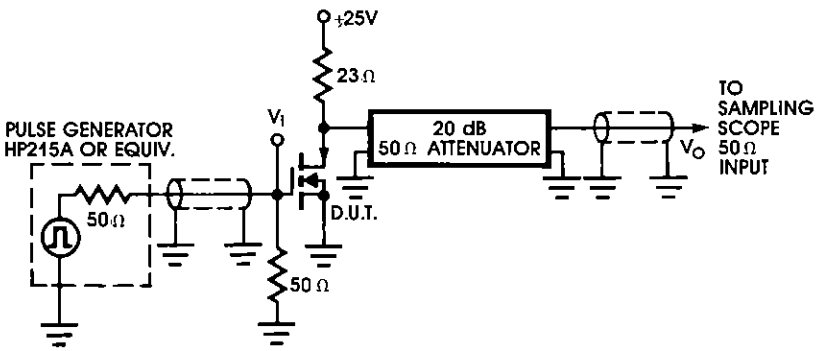
Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
BV_{DSS}	Drain-Source Breakdown Voltage	30			V	V_{GS}=0, I_D=100µA
$V_{GS}(th)$	Gate-Source Threshold Voltage	0.8			V	V_{GS}=V_{DS}, I_D=1mA
I_{GSS}	Gate Leakage Current			10	µA	V_{GS}=12V, V_{DS}=0, T_A=80°C
I_{DSS}	Drain Leakage Current			500	µA	V_{GS}=0, V_{DS}=24V, T_A=80°C
$r_{DS}(N)$	N-Channel On-Resistance (Note 1)			1.0	Ω	V_{GS}=10V, I_D=1A, T_A=25°C
$r_{DS}(P)$	P-Channel On-Resistance (Note 1)			2.0	Ω	V_{GS}=10V, I_D=1A, T_A=25°C

Note: 1. Pulse test — 80µs pulse, 1% duty cycle. r_{DS} increase 0.6%/°C.

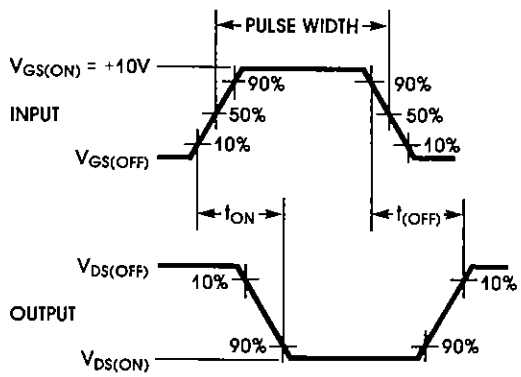
A.C. Characteristics T_A=25°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{ON}(N)	N-Channel Turn-On Time			20	ns	See Switching Time Test Circuit and Waveforms below
t_{ON}(P)	P-Channel Turn-On Time			30	ns	
t_{OFF}(N)	N-Channel Turn-Off Time			20	ns	
t_{OFF}(P)	P-Channel Turn-Off Time			30	ns	

Switching Time Test Circuit



Switching Time Test Waveforms



Capacitance T_A=25°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{iss}(N)	N-Channel Input Capacitance			175	pF	V_{GS}=0, V_{DS}=12V, f=1MHz
C_{iss}(P)	P-Channel Input Capacitance			190	pF	V_{GS}=0, V_{DS}=12V, f=1MHz

Absolute Maximum Ratings*

Temperature Under Bias ..... -20° to +80°C
Storage Temperature ..... -40° to +150°C
Drain Voltage (with respect to Gate or Source) 30V
Continuous Drain Current 2A
Peak Drain Current 3A
Power Dissipation (T_A=80°C) 1.05W
Power Dissipation (T_A=25°C) 1.75W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.